AD1452 Brief

Latest Version: V2.3

Declaration

Disclaimer

Information given in this document is provided just as a reference or example for the purpose of using DashChip's products, and cannot be treated as a part of any quotation or contract for sale. DashChip products may contain design defects or errors known as anomalies or errata which may cause the products' functions to deviate from published specifications. Designers must not rely on the instructions of DashChip's products marked "Reserved" or "undefined". DashChip reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

DASHCHIP DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL EXPRESS OR IMPLIED WARRANTIES OF MERCHANTABILITY, ACCURACY, SECURITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY AND THE LIKE TO THE INFORMATON OF THIS DOCUMENT AND DASHCHIP PRODUCTS.

IN NO EVENT SHALL DASHCHIP BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES WHATSOEVER, INCLUDING, WITHOUT LIMITATION FOR LOST OF DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND ARISING FROM USING THE INFORMATON OF THIS DOCUMENT AND DASHCHIP PRODUCTS. REGARDLESS OF THE FORM OF DASHCHIP WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF DASHCHIP OR OTHERS; STRICT LIABILITY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER DASHCHIP HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES OR NOT.

DashChip's products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an officer of DashChip and further testing and/or modification will be fully at the risk of the customer.

Ways of obtaining information

Copies of this document and/or other DashChip product literature, as well as the Terms and Conditions of Sale Agreement, may be obtained by visiting DashChip's website at: http://www.dash-chip.com or from an authorized DashChip representative.

Trademarks

The word “DashChip”, the logo and Word “炬迪” are the trademark of DashChip Technology Co., Ltd. Names and brands of other companies and their products that may from time to time descriptively appear in this document are the trademarks of their respective holders, no affiliation, authorization, or endorsement by such persons are claimed or implied except as may be expressly stated therein.

Rights Reserved

The provision of this document shall not be deemed to grant buyers any right in and to patent, copyright, trademark, trade secret, know how, and any other intellectual property of DashChip or others.

Miscellaneous

Information contained or described herein relates only to the DashChip products and as of the release date of this publication, abrogates and supersedes all previously published data and specifications relating to such products provided by DashChip or by any other person purporting to distribute such information.

DashChip preserves the rights to make changes to information described herein at any time without notice. Please contact your DashChip sales representatives to obtain the latest information before placing your product order.

Additional Support

Additional products and company information can be obtained by visiting the DashChip website at: http://www.dash-chip.com

Revision History

Version	Contents	Date
V1.0	Initial version.	2024-1-24
V1.1	Fixed PIN order error in PIN assignment diagram	2024-3-12
V1.2	External SPI NorFlash is supported by default, and PIN3 is fixed to the power supply Modify the initial state of GPIO5/6/8/9/10/11/15	2024-5-16
V1.4	Modify ordering information Modify pin assignment diagram	2024-11-6
V1.5	Modify ordering information	2024-11-13
V1.6	Modify ordering information	2025-2-15
V1.8	Add electrical characteristics	2025-3-3
V2.0	Modify PIN Description (pin2 to GND) Add ADC/DAC filter parameter Modify ADC/DAC performance parameter	2025-5-11
V2.2	Modify power consumptions	2025-6-17
V2.3	Modified audio ADC pass band ripple parameter Modified audio DAC pass band ripple parameter	2025-8-2

1 Introduction

The AD1452 is a highly integrated DSP (Digital Signal Processor) for audio system. The AD1452 integrates a Xtensa-HIFI4 audio DSP with FPU, including up to 2 channels D-MIC interface with decimation filters, and 2 channels A-MIC with high performance ADC, stereo high performance DAC. It integrates two I2S/TDM compatible audio interfaces, which can support 32 channels input and 32 channels output. It also integrates a high-performance ASRC with 8 channels, and THD+N is less than -140dB. The AD1452 is a MCU-less chip, and the main MCU loads DSP codes and configuration registers to AD1452 through the I2C/SPI slave mode interface. In ChipSlave mode, the DSP can be run according to the RAM address configured by the MCU, and in ChipMaster mode, the DSP can be started directly from BROM+SPINOR.

1.1 Key Features

■ *DSP*

- VLIW & SIMD Architecture Xtensa-HIFI4 Audio DSP with FPU, up to 294.912MHz.
- Support four 32x32-bit MACs or eight 32x16-bit MACs or eight 16x16-bit MACs.
- Support 72-bit accumulators.
- Provide up to four single-precision IEEE floating point MACs per cycle.
- Support fourth VLIW slot and the ability to issue two 64-bit loads per cycle.
- Support Vector floating-point precision support for enhanced audio and voice processing.
- Support 96KB IRAM and 256KB DRAM, programmable, shareable.

- Compatible at the C/C++ source level for the programs optimized using intrinsic.

■ *DMA*

- Support memory-to-memory, memory-to-peripheral, and peripheral-to-memory.
- Provide 16-channel ordinary DMA that supports for transmission in burst 8 mode or single mode.
- Transmission width includes 8-bit, 16-bit, and 32-bit.
- Support separated mode for audio.

■ *μP Interface*

- Support SPI slave, up to 40MHz.
- Support I2C salve standard mode (100kbps), fast-speed mode (400kpbs) and super-fast-speed mode (1Mpbs) The default slave address is 0xCC, and support configuring the slave address register to change the slave address by the I2C interface.
- Support Burst/Single mode Read/Write.
- Support Read/Write the I/DRAM while DSP running.

■ *Audio ADC*

- Built-in stereo 24bit input sigma-delta ADCs, SNR (A-WEIGHTING): 115dB, THD+N: -93dB.
- The input source can be selected from MIC amplifiers and Auxin.
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz.

- A digital high-pass filter can be used to remove DC offsets, and its cut-off frequency is configured.
- There are seven different frequency response curves low-pass filter can be selected for voice, sound or music application.
- Support automatic amplitude limitation.
- Support single-ended input analog microphones and stereo full difference input microphones.
- Support 2 channels PDM Digital microphones.

■ *Audio DAC*

- Built-in stereo 24bit sigma-delta DAC, SNR (A-WEIGHTING): 120dB, THD+N: -100dB.
- DAC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz.
- Support digital volume of 256 steps with zero cross detection.
- Support differential audio output for speaker PA.
- Full-scale output voltage. The output voltage is proportional to 1Vrms (Single mode) and 2Vrms (Differential mode).
- Support sample counter function.

■ *ASRC*

- Four audio sample rate converter (expandable up to 8 channels), support SSRC, ASRC, PHASE mode.

- THD+N: <=-140dB (for all common conversion ratios).
- Flexible input and output interfaces. TDM, I2S, ADC, DAC or SRAM.
- Support automatically adjusting to changes in both input and output sample rates.
- Latency: 16~64/FSin+2/FSout.
- High input jitter tolerance: support occasional bursts or skips of a couple of samples without sacrificing quality in practical terms.
- Input sample rate range:

  8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96k/176.4k/192kHz.
- Output sample rate range:

  8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96k/176.4k/192kHz.
- Sampling rate conversion ratios: 2:1 to 1:24.
- Support mute and Fade in/out.
- Support bypass mode.

■ *I2S*

- 2 groups of fully functional I2STX.
- 2 groups of fully functional I2SRX.
- Each group fully functional I2S supports 1/2/4/8/16 channels.
- Support multiple data lines(2D~8D) or single data line(1D), Formats: Stardard/L-J/R-J.
- Support TDM4/TDM8/TDM16
- Support DSP mode (max @ 4channel).
- Support PCM Short /Long frame synchronization.

- Support master/slave mode.
- Support I2S slave mode sampling rate change & channel width change & timeout detection.
- Support synchronization or asynchronization LRCLK&BCLK @ master/slave mode.
- Data size supports 16/20/24/32-bit.
- Sampling rate supports 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96k/192k/384k (Bclk max @ 24.576MHz).
- Channel width supports 16 or 32 BCLK cycles.
- Bit order supports MSB/LSB.
- LRCLK pulse width supports 1/16/32 BCLK width or 50% duty of LRCLK cycle width.
- MCLK, BCLK, LRCLK output independent gating.
- BCLK phase inversion.

■ *UART*

- One on-chip UART Controllers inside.
- Support 3.3v and 1.8v.
- 5-8 Data Bits and LSB first in Transmit and Received.
- 1-2 Stop Bits.
- Even, Odd or No Parity.
- Capable of speeds 400bps to 6Mbps to enable connections with Bluetooth and other peripherals.
- Support IRQ and DMA mode to transmit data.

- RX Baud Rate tolerance≤±2%.

■ *I2C*

- Two on-chip I2C controllers inside.
- Support 3.3v and 1.8v.
- Both master and slave functions support.
- Both master and slave supports DMA mode.
- Support standard mode (100kbps), fast-speed mode (400kbps), super-fast-speed mode (1Mbps).
- Multi-slave capability.
- 7-bit address mode support.

■ *SPI*

- Support SPI normal mode: Mode 0\1\2\3.
- Support standard SPI, Dual SPI, Quad SPI.
- Support normal 3 wire mode.
- Support IRQ and DMA mode to transmit data.
- Support 32 level delay chain, 0.5ns/step.
- Master mode and slave mode.
- Support 50MHz *spi_clk* as highest speed.

■ *System*

- Support SPI NOR boot, up to 50MHz.
- AVCC support 3.0~3.6V external power supply.
- IOVCC support 1.7~3.6V external power supply.
- Internal LDO output VDD from AVCC.
- Internal 32k&64M RC from AVCC.
- Support oscillator inputs: HOSC(24.576MHz).
- Supply Audio PLL and DSP PLL, the sources of the PLLs are HOSC or Bclk.
- Flexible general purpose 31 IOs.
- Timer*2.
- Watchdog

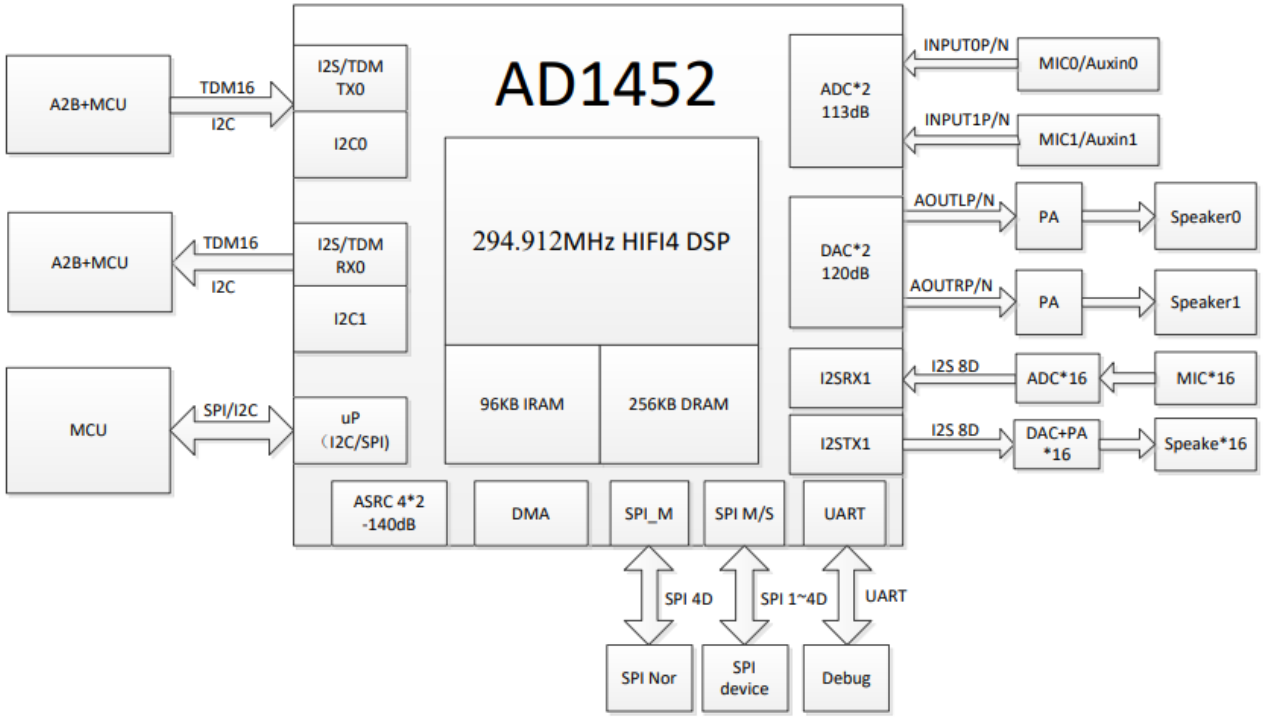
■ *Package and Ordering Information*

Minimum Order Quantity: 1600EA

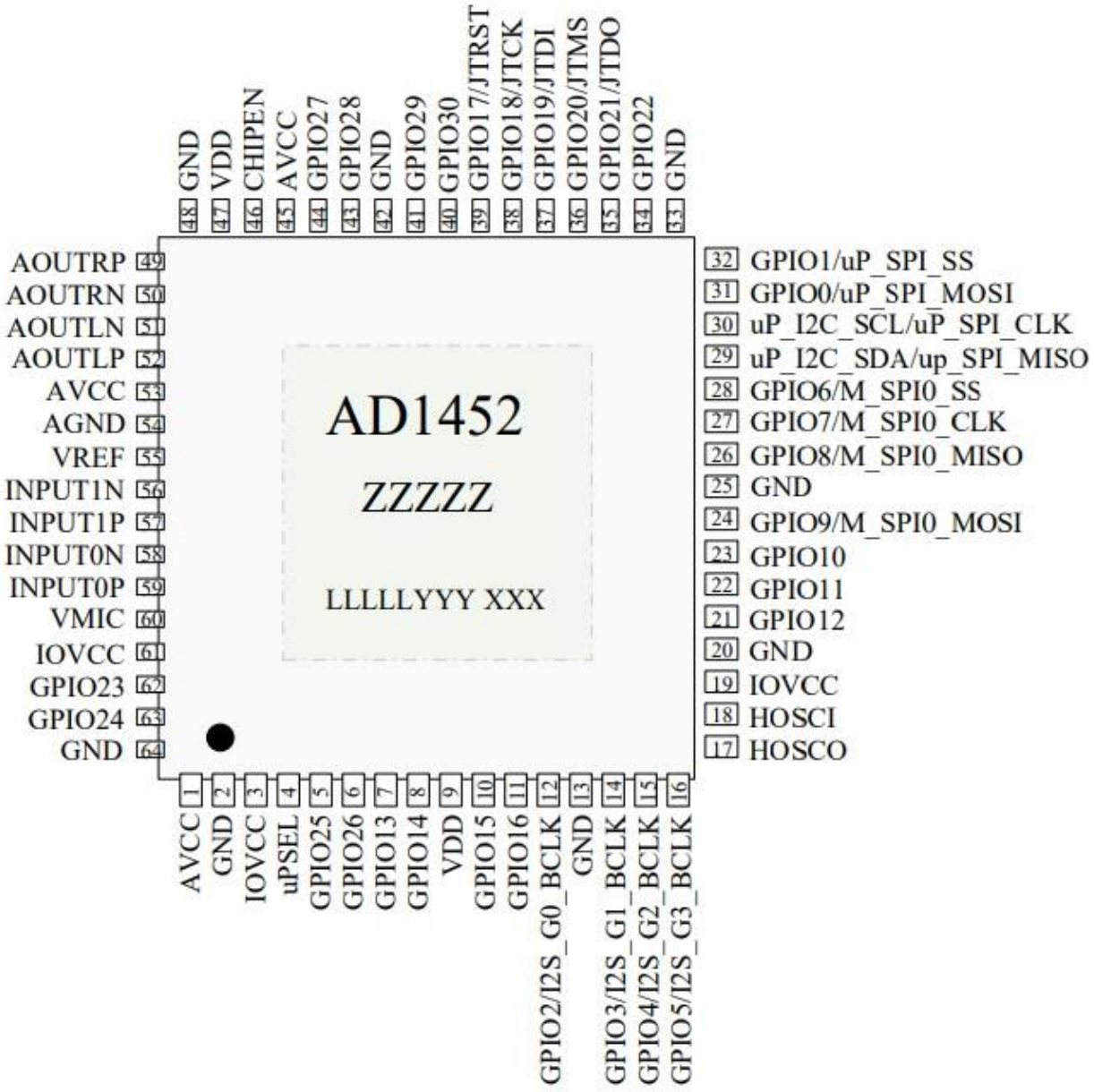
Packaging Form: Tray

Part Number	Ta	Feature Code	Package	Package Size
AD1452C1SWA	0~70℃	Consumer	E-PAD LQFP64L	10mm x 10mm x 1.6mm
AD1452A2SWA	-40~85℃	Industrial	E-PAD LQFP64L	10mm x 10mm x 1.6mm
AD1452A3SWA	-40~105℃	Automotive	E-PAD LQFP64L	10mm x 10mm x 1.6mm

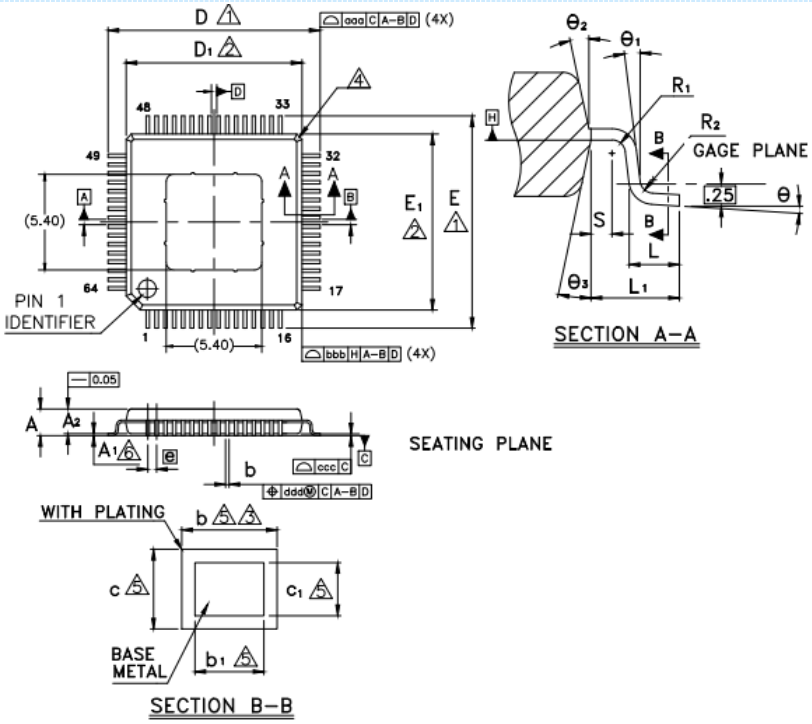
1.2 Block Diagram



1.3 PIN Assignment



1.4 Package Drawing



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.025	—	0.127	0.001	—	0.005
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	11.85	12.00	12.15	0.467	0.472	0.478
D_1	9.90	10.00	10.10	0.390	0.394	0.398
E	11.85	12.00	12.15	0.467	0.472	0.478
E_1	9.90	10.00	10.10	0.390	0.394	0.398
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

1.5 AD1452 PIN Description

PIN No.	PIN Name	PIN Description	GPIO Initial State
1	AVCC	Analog Power Supply PIN (3.0~3.6V)	
2	GND	Ground PIN 0V	
3	IOVCC	Digital IO Power Supply Pin（1.7~3.6V）	
4	uPSEL	MCU Slave Interface Select Pin uPSEL pin="L": SPI Interface uPSEL pin="H": I2C Interface The uPSEL pin must be fixed to "L"(GND) or "H"(IOVCC)	L
5	GPIO25	MFP1[Note]	Z
6	GPIO26	MFP1[Note]	Z
7	GPIO13	MFP1[Note] (JTAG_CTL="0x10",the PIN is JTCK)	Z
8	GPIO14	MFP1[Note] (JTAG_CTL="0x10",the PIN is JTDI)	Z

9	VDD	Power Supply PIN for Digital Core	
10	GPIO15	MFP1[Note] (JTAG_CTL="0x10",the PIN is JTMS)	*
11	GPIO16	MFP1[Note] (JTAG_CTL="0x10",the PIN is JTDO)	Z
12	GPIO2	MFP0[Note] and best recommendation for I2S_G0_BCLK input	Z
13	GND	Ground PIN 0V	
14	GPIO3	MFP0[Note] And best recommendation for I2S_G1_BCLK input	Z
15	GPIO4	MFP0[Note] And best recommendation for I2S_G2_BCLK input	Z
16	GPIO5	MFP0[Note] And best recommendation for I2S_G3_BCLK input	Z
17	HOSCO	Crystal Oscillator Output PIN When a crystal oscillator is used, connect it between HOSCI and HOSCO. When a crystal oscillator is not used, leave this pin as open	
18	HOSCI	Crystal Oscillator Input PIN When a crystal oscillator is used, connect it between HOSCI and HOSCO. When a crystal oscillator is not used, connect this pin to the external clock or leave open	
19	IOVCC	Digital IO Power Supply PIN (1.7~3.6V)	
20	GND	Ground PIN 0V	
21	GPIO12	MFP0[Note] (JTAG_CTL="0x10",the PIN is JTRST)	Z
22	GPIO11	MFP0[Note]	*
23	GPIO10	MFP0[Note]	*
24	GPIO9	M_SPI0_MOSI/MFP0[Note]	*
25	GND	Ground PIN 0V	
26	GPIO8	M_SPI0_MISO/MFP0[Note]	*
27	GPIO7	M_SPI0_CLK/MFP0[Note]	*
28	GPIO6	M_SPI0_SS/MFP0[Note]	*
29	I2C_SDA	uP_ SPI_MISO(uPSEL="L") and uP_I2C_SDA(uPSEL="H")	ZH
30	I2C_SCL	uP_SPI_CLK(uPSEL="L")and uP_I2C_SCL(uPSEL="H")	ZH
31	GPIO0	uP_SPI_MOSI (uPSEL="L") and MFP0[Note](uPSEL="H")	Z
32	GPIO1	uP_SPI_SS (uPSEL="L") and MFP0[Note](uPSEL="H")	Z
33	GND	Ground PIN 0V	
34	GPIO22	MFP1[Note]	Z
35	GPIO21	MFP1[Note] (JTAG_CTL="0x11"(default),the PIN is JTDO)	L
36	GPIO20	MFP1[Note] (JTAG_CTL="0x11"(default),the PIN is JTMS)	H
37	GPIO19	MFP1[Note] (JTAG_CTL="0x11"(default),the PIN is JTDI)	H

38	GPIO18	MFP1[Note] (JTAG_CTL="0x11"(default),the PIN is JTCK)	H
39	GPIO17	MFP0[Note] (JTAG_CTL="0x11"(default),the PIN is JTRST)	H
40	GPIO30	MFP1[Note]	Z
41	GPIO29	MFP1[Note]	Z
42	GND	Ground PIN 0V	
43	GPIO28	MFP1[Note]	Z
44	GPIO27	MFP1[Note]	Z
45	AVCC	Analog Power Supply PIN (3.0~3.6V)	
46	CHIPEN	CHIP enable CHIPEN pin="L": Reset CHIPEN pin="H": Normal Run	
47	VDD	Power Supply PIN for Digital Core	
48	GND	Ground PIN 0V	
49	AOUTRP	DAC Output PIN	
50	AOUTRN	DAC Output PIN	
51	AOUTLN	DAC Output PIN	
52	AOUTLP	DAC Output PIN	
53	AVCC	Analog Power Supply PIN (3.0~3.6V)	
54	AGND	Analog Ground PIN 0V	
55	VREF	Analog Reference Voltage	
56	INPUT1N	ADC Input PIN, MFP2[Note]	Z
57	INPUT1P	ADC Input PIN, MFP2[Note]	Z
58	INPUT0N	ADC Input PIN, MFP2[Note]	Z
59	INPUT0P	ADC Input PIN, MFP2[Note]	Z
60	VMIC	MIC Bias Power Supply PIN	
61	IOVCC	Digital IO Power Supply PIN (1.7~3.6V)	
62	GPIO23	MFP1[Note]	Z
63	GPIO24	MFP1[Note]	Z
64	GND	Ground PIN 0V	

- **Note:**

Z: High resistance.

H: High.

*****: Infinitive.

L: Low.

- **Note1: MFP0**

0: GPIOx	21: I2STX0_D0	42: I2SRX0_D5
1: SPI0_SS	22: I2STX0_D1	43: I2SRX0_D6
2: SPI0_CLK	23: I2STX0_D2	44: I2SRX0_D7
3: SPI0_MISO	24: I2STX0_D3	45: I2SRX1_D0
4: SPI0_MOSI	25: I2STX0_D4	46: I2SRX1_D1
5: SPI0_D2	26: I2STX0_D5	47: I2SRX1_D2
6: SPI0_D3	27: I2STX0_D6	48: I2SRX1_D3
7: UART_TX	28: I2STX0_D7	49: I2SRX1_D4
8: UART_RX	29: I2STX1_D0	50: I2SRX1_D5
9: I2S_G0_MCLK	30: I2STX1_D1	51: I2SRX1_D6
10: I2S_G1_MCLK	31: I2STX1_D2	52: I2SRX1_D7
11: I2S_G2_MCLK	32: I2STX1_D3	53: DMIC_CLK
12: I2S_G3_MCLK	33: I2STX1_D4	54: DMIC_DAT
13: I2S_G0_LRCLK	34: I2STX1_D5	55: STO

14: I2S_G1_LRCLK	35: I2STX1_D6	56: AEC_I2STX5_D0
15: I2S_G2_LRCLK	36: I2STX1_D7	57: I2C0_CLK
16: I2S_G3_LRCLK	37: I2SRX0_D0	58: I2C0_DAT
17: I2S_G0_BCLK	38: I2SRX0_D1	59: I2C1_CLK
18: I2S_G1_BCLK	39: I2SRX0_D2	60: I2C1_DAT
19: I2S_G2_BCLK	40: I2SRX0_D3	
20: I2S_G3_BCLK	41: I2SRX0_D4	

- **MFP1 (The only difference from MFP0 is SPI1 function instead of SPI0)**

0: GPIOx	21: I2STX0_D0	42: I2SRX0_D5
1: SPI1_SS	22: I2STX0_D1	43: I2SRX0_D6
2: SPI1_CLK	23: I2STX0_D2	44: I2SRX0_D7
3: SPI1_MISO	24: I2STX0_D3	45: I2SRX1_D0
4: SPI1_MOSI	25: I2STX0_D4	46: I2SRX1_D1
5: SPI1_D2	26: I2STX0_D5	47: I2SRX1_D2
6: SPI1_D3	27: I2STX0_D6	48: I2SRX1_D3
7: UART_TX	28: I2STX0_D7	49: I2SRX1_D4
8: UART_RX	29: I2STX1_D0	50: I2SRX1_D5

9: I2S_G0_MCLK	30: I2STX1_D1	51: I2SRX1_D6
10: I2S_G1_MCLK	31: I2STX1_D2	52: I2SRX1_D7
11: I2S_G2_MCLK	32: I2STX1_D3	53: DMIC_CLK
12: I2S_G3_MCLK	33: I2STX1_D4	54: DMIC_DAT
13: I2S_G0_LRCLK	34: I2STX1_D5	55: STO
14: I2S_G1_LRCLK	35: I2STX1_D6	56: AEC_I2STX5_D0
15: I2S_G2_LRCLK	36: I2STX1_D7	57: I2C0_CLK
16: I2S_G3_LRCLK	37: I2SRX0_D0	58: I2C0_DAT
17: I2S_G0_BCLK	38: I2SRX0_D1	59: I2C1_CLK
18: I2S_G1_BCLK	39: I2SRX0_D2	60: I2C1_DAT
19: I2S_G2_BCLK	40: I2SRX0_D3	
20: I2S_G3_BCLK	41: I2SRX0_D4	

- **MFP2 (Less reuse functional than MFP0 and MFP1)**

	INPUT0N	**INPUT0P**	**INPUT1N**	**INPUT1P**
0:	GPIO32	GPIO33	GPIO34	GPIO35
53:	DMIC_CLK	DMIC_CLK	DMIC_CLK	DMIC_CLK

54:	DMIC_DAT	DMIC_DAT	DMIC_DAT	DMIC_DAT
63:	INPUT0N	INPUT0P	INPUT1N	INPUT1P

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

These absolute maximum ratings are stress ratings, operating at or beyond these ratings for extended periods of time (above 1ms) may result in permanent damage to the AD1452. Unless specified, all voltages are relative to VSS.

Table 2-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	IOVCC	-0.3	3.3	3.6	V
	AVCC	-0.3	3.3	3.6	V
	VDD	-0.3	1.15	1.3	V
Input Voltage	IO	-0.3	IOVCC	IOVCC+0.3	V
ESD-Human body model	HBM	2000			V
ESD-Charged Device Model	CDM	500			V
Thermal Resistance(Junction to Case)	Θjc		6.9		°C/W
Thermal Resistance(Junction to Ambient)	Θja		21.3		°C/W
Ambient Temperature[note]	Tamb	-40	25	105	°C
Storage temperature	Tstg	-55		+150	°C

Note:

1. Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum

ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

2. All voltage values are relative to GND.

3. Θja ,Θjc: JEDEC 2S2P PCB, Power consumption: 115mw in typical case.

2.2 Recommended Operating Conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 2-2 Recommended Operating Conditions

Supply Voltage	Min	Typ	Max	Unit
IOVCC	1.7	3.3	3.6	V
AVCC	3.0	3.3	3.6	V
VDD	1.0	1.15	1.3	V

2.3 DC Characteristics

Table 2-3 DC Parameters for +3.3V IO Pin With Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.8	V	VCC = 3.3V
High-level input voltage	VIH	2.0	-	V	
Low-level output voltage	VOL	-	0.4	V	
High-level output voltage	VOH	2.4	-	V	

Table 2-4 DC Parameter for +3.3V IO Pin With Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition
Schmitt trigger positive-going threshold	VT+	-	1.9	V	VCC=3.3V
Schmitt trigger negative-going threshold	VT-	1.2	-	V	

Table 2-5 DC Parameters for +1.8V IO Pin With Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.4	V	VCC = 1.8V
High-level input voltage	VIH	1.2	-	V	
Low-level output voltage	VOL	-	0.36	V	
High-level output voltage	VOH	1.4	-	V	

Table 2-6 DC Parameter for +1.8V IO Pin With Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition
Schmitt trigger positive-going threshold	VT+	-	1.1	V	VCC=1.8V
Schmitt trigger negative-going threshold	VT-	0.7	-	V	

2.4 Power Consumptions

Table 2-7 Power Consumption Table

	Symbol	MIN.	TYP.	MAX.	Unit
Active: DSP is running (**FFT_R32x32_N512,VDD:1.15V,AVCC=3.3V IOVCC=3.3V, 25℃**)	I_{IOVCC}		10	50	mA
	I_{AVCC}		10	50	mA
	I_{VDD}		10+0.35mA/MHz*dspclk 115（dspclk is about 300MHz）	200	mA
Idle Only for RAM contention	$I_{wholechip}$		1.5	5	mA
Powerdown CHIPEN pin= “L”	$I_{wholechip}$		0.5		uA

2.5 Digital Filter Characteristics

2.5.1 ADC

Table 2-8 Audio ADC Performance Parameters (Differential Mode)

48kfs Differential 0db Gain, 5kR input res, 27℃ temperature				
Characteristics	**MIN.**	**TYP.**	**MAX.**	**Unit**
Noise	-	2.24	-	uFFS
Noise(A-Weighting)	-	1.78	-	uFFS
SNR(THD+N < 1%)	110	113	-	dB
SNR(THD+N < 1%, A-Weighting)	112	115	-	dB
Dynamic Range(Input= –60dBFS@1kHz)	110	113	-	dB
Dynamic Range(Input= –60dBFS@1kHz, A-weighting)	112	115	-	dB
THD+N(-3dbFS)		-93	-90	dB
THD+N(-3dbFS) (A weighting)		-93	-90	dB
Input Common Mode Voltage	-	1.5	-	V
Full Scale Input Voltage(THD+N = 1%)	-	2.2	-	Vrms
IMD	-	-84	-	dB
Crosstalk	-	-120	-	dB
Channel Gain Deviation	-	0.1	-	dB
Channel Phase Deviation	-	0	0.005	deg

Table 2-9 Audio ADC Performance Parameters (Single-ended Mode)

48kfs single-ended 0db Gain, 5kR input res, 27℃ temperature				
Characteristics	**MIN.**	**TYP.**	**MAX.**	**Unit**
Noise	-	3.35	-	uFFS
Noise(A-Weighting)	-	2.66	-	uFFS
SNR(THD+N < 1%)	106	109	-	dB
SNR(THD+N < 1%, A-Weighting)	108	111	-	dB
Dynamic Range(Input= –60dBFS@1kHz)	106	109	-	dB

Dynamic Range(Input= –60dBFS@1kHz, A-weighting)	109	112	-	dB
THD+N(-3dbFS)		-87	-80	dB
THD+N(-3dbFS) (A weighting)		-87	-80	dB
Input Common Mode Voltage	-	1.5	-	V
Full Scale Input Voltage(THD+N = 1%)	-	1.1	-	Vrms
IMD	-	-78	-	dB
Crosstalk	-	-120	-	dB
Channel Gain Deviation	-	0.1	-	dB
Channel Phase Deviation	-	0	0.005	deg

ADC Decimation Filter						
Parameter	Conditions		Min	Typ	Max	Unit
Pass Band	typical at fs = 48 kHz	0.453 × fs		21.74		kHz
Pass Band Ripple			-0.06		0.06	dB
Transition Band		0.5 × fs		24		kHz
Stop Band		0.506 × fs		24.288		kHz
Stop Band Attenuation			70			dB
Group Delay		33.5/fs	698			us

2.5.2 DAC

Table 2-10 Audio DAC Performance Parameters (Differential Mode)

48kfs Differential 0db				
Characteristics	MIN.	TYP.	MAX.	Unit
Noise	-	2.3	-	uV
Noise(A-Weighting)	-	2	-	uV
SNR	115	118	-	dB
SNR(A-Weighting)	117	120	-	dB
Dynamic Range(Input= –60dBFS@1kHz)	115	118	-	dB
Dynamic Range(Input= –60dBFS@1kHz, A-weighting)	117	120	-	dB
THD+N(0dBFS@1khz)	-	-100	-92	dB
THD+N(A weighting)(0dBFS@1khz)	-	-100	-92	dB
THD+N(-1dBFS@1khz)	-	-100	-92	dB
THD+N(A weighting)(-1dBFS@1khz)	-	-100	-92	dB
Max Output Amplitude	-	2	-	Vrms
Max Output Power	-	-	-	mW
IMD	-	-94	-	dB
Crosstalk	-	-110	-	dB

Table 2-11Audio DAC Performance Parameters (**S**ingle-ended Mode)

48kfs single-ended 0db				
Characteristics	MIN.	TYP.	MAX.	Unit
Noise	-	2.45	-	uV
Noise(A-Weighting)	-	1.9	-	uV
SNR	109	112	-	dB
SNR(A-Weighting)	111	114	-	dB
Dynamic Range(Input= –60dBFS@1kHz)	108	111	-	dB
Dynamic Range(Input= –60dBFS@1kHz, A-weighting)	110	113	-	dB
THD+N(0dBFS@1khz)	-	-97	-90	dB
THD+N(A weighting)(0dBFS@1khz)	-	-97	-90	dB
THD+N(-1dBFS@1khz)	-	-97	-90	dB

THD+N(A weighting)(-1dBFS@1khz)	-	-97	-90	dB
Max Output Amplitude	-	1	-	Vrms
Max Output Power	-	-	-	mW
IMD	-	-90	-	dB
Crosstalk	-	-103	-	dB

DAC Interpolation Filter						
Parameter	Conditions		Min	Typ	Max	Unit
Pass band	Typical at fs=48kfs	0.419 × fs		20.1		Khz
Pass band ripple			-0.01		+0.01	dB
Transition band(-3db)		0.44375 × fs		21.3		Khz
Stop band		0.5 × fs		24		Khz
Stop band attenuation			99			dB
Group delay		35/fs		729		us

2.6 ASRC Performance

Table 2-12 ASRC Performance Parameters

In rate->out rate	THD+N(dB)		RMS Level(dBFS)	F(Cut-off)Hz(-3db pos)
8k->48k	1khz:	-142 db	+/-0.005 dBFS	
	Sweep:	-141 db		3.7khz
11.025k->48k	1khz:	-142 db	+/-0.005 dBFS	
	Sweep:	-141 db		5.2khz
12k->48k	1khz:	-142 db	+/-0.005 dBFS	
	Sweep:	-141 db		5.6khz
16k->48k	1khz:	-143 db	+/-0.005 dBFS	
	Sweep:	-140 db		7.5khz
22.05k->48k	1khz:	-141 db	+/-0.005 dBFS	
	Sweep:	-140 db		10.3khz
24k->48k	1khz:	-140 db	+/-0.005 dBFS	
	Sweep:	-140 db		11.2khz
32k->48k	1khz:	-142 db	+/-0.005 dBFS	
	Sweep:	-140 db		14.9khz
44.1k->48k	1khz:	-141 db	+/-0.005 dBFS	
	Sweep:	-141 db		20.5khz
48k->48k	1khz:	-144 db	+/-0.005 dBFS	
	Sweep:	-143 db		22.5khz

96k->48k	1khz:	-144 db	+/-0.005 dBFS	
	Sweep:	-144 db		21.9khz
48k->44.1k	1khz:	-142 db	+/-0.005 dBFS	
	Sweep:	-141 db		20.8khz
8k->96k	1khz:	-142 db	+/-0.005 dBFS	
	Sweep:	-140 db		3.7khz

2.7 DSP Performance

Table 2-13 DSP Performance Parameters

VDD	Max(MHz)	GMACs(32bit)	GFLOPS(SP)
1.10V	184.32	0.74	1.47
1.20V	258.048	1.03	2.06
1.25V	294.912	1.18	2.36

DashChip Technology Co., Ltd.

Address: Room 401, 4th Floor, Building 4, Lane 88, Haiyang 2nd Road, Lingang New Area, China (Shanghai) Pilot Free Trade Zone

http://www.dash-chip.com

Business Email: mp-sales@dash-chip.com

Technical Service Email: mp-cs@dash-chip.com